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HIGHLY ACCURATE DESIGN OF SPIRAL INDUCTORS FOR MMIC's WITH SMALL SIZE AND HIGH CUT-OFF FREQUENCY CHARACTERISTICS

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ABSTRACT :

High precision experimental and theoretical procedures are presented for obtaining very compact inductors (diameter 80 to 200 μm) with values up to 5 nH and cut-off frequencies ranging from 20 to 100 GHz for L < 2 nH.

The maximum phase and amplitude measurement error is of the order to ± 2 degrees and 1% respectively with typical measurement reproducibility of 0.1%. A new lumped element theory is presented predicting the electrical characteristics of spiral inductors with a maximum error of only 5%.

INTRODUCTION

Spiral inductor characteristics reported in the litterature take no account of the ground plane influence (1) wich is very important in case of thinned (100 μm) MMIC substrates, and correspond to components occupying prohibitively large MMIC area (1,2). The maximum design errors of 15% reported for the above inductors are not acceptable for MMIC design where the tolerance in the design element values shoud be much smaller to avoid considerable circuit performance deterioration. We report here on high precision experimental and theoretical procedures for obtaining very compact inductors with excellent electrical characteristics.

THEORETICAL ANALYSIS AND MODELLING

The theory presented here predicts the frequency response of spiral inductors with circular or rectangular geometries. It considers the dielectric substrate influence and ground plane effects. The metallisation thickness (t) is assumed to be small with respect to the turn width (W).

For the purpose of the analysis, spiral inductors with N turns (N = integer) are divided into N elementary circuits connected in series and having circular or rectangular geometries. The mutual inductance and capacitance of every turn is determined by treating the turns as lumped elements.

An electrostatic approach is used to evaluate the mutual capacitive coefficients C_{ij} between two turns i and j. Each turn is divided into n elementay turns of smaller width, each with a uniform charge distribution. The electrostatic potential at any point of the surface is given by a Green function which takes into account the air-dielectric interface and the ground plane. An analytic formula could be derived for this potential due to the circular symmetric shape of the spirals. Following this derivation we fix the potential of turn i to 1 Volt while maintaining all other turns at 0 Volt . The charges of all other conductors and consequently the coefficients C_{ij} can then be evaluated by solving the resulting system of n * N linear equations.

A similar approach based on magnetostatic theory is used in order to obtain the inductive coefficients L_{ij} of the different turns. A uniform current is assumed to circulate along each turn. Its density across the turn is however variable and depends on the charge distribution. Ground plane effects are considered by introducing in the calculation the image of each turn with respect to the plane. By using the Neumann formula :

$$L_{ij} = \frac{\mu o}{4\pi} \int \frac{\vec{dl}i.\vec{dl}j}{r}$$

one obtains simple expressions for circular turns or for rectangular geometries with any finite dimension .

Given the values of the C_{ij} and L_{ij} coefficients of the elementary circuits (turns), we can now evaluate the frequency response of the total network (spiral inductor). The potential difference $V_k - V_{k+1}$ across the spiral turn K defined between nodes and K + 1 is due to its mutual inductance L_{kj}, as well as, to its resistance R_k :

$$V_K - V_{K+1} = \sum_{j=1}^{n} i\, L_{jk}\, \omega \left(\frac{I_j + I_{j+1}}{2}\right) + R_K \left(\frac{I_K + I_{K+1}}{2}\right)$$

Similarly the current difference is due to the capacitive influence with the other turns and is given by :

$$I_K - I_{K+1} = \sum_{j=1}^{N} i\, C_{jk}\, \omega \left(\frac{V_K + V_{K+1}}{2}\right)$$

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The average current (or potential) across a turn is assumed to be equal to the average of the currents (or potentials) at its two ends. By fixing the currents I_1 , I_{N+1} at the spiral ends we obtain a system of 2 N equations, the solution, of which gives the potentials V_1, V_{N+1} of the two port. The impedance matrix (Z) and subsequently the scattering matrix (S) can then be evaluated at different frequencies.

The presented theory is valid for "lumped" elementary turns. The "lumped" element condition is satisfied for spiral diameters (d) and substrate thickness (h) much smaller than the wavelength (λ) : $d \ll \lambda$, $h \ll \lambda$. This is certainly true for MMIC's on 100 µm substrates and spirals with diameters not exceeding 200 µm.

Individual turns are treated as lumped elements, but the whole inductance looks like a distributed network. This implies that the total spiral length can be a considerable fraction of λ. The theories presented up to now treat spiral inductors as a set of coupled line segments. These segments should be straight lines of relatively long length compared to the substrate thickness. In contrast to other theories, our approach allows the exact evaluation of circular geometries and the study of components with dimensions of the same order of magnetude as the thickness h.

The results obtained by our theory could be very well fitted by a simple equivalent circuit Fig 1 :

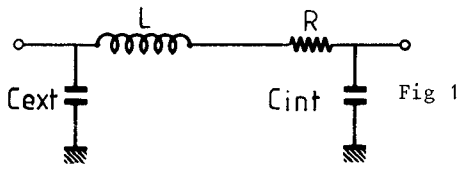

Fig 1

The circuit consists of an inductor in series with a resistance and in parallel with parasitic capacitances to ground. Their values have been obtained by a "least square" optimisation program which minimises the squares of the difference between theoretical and modeled S-parameter values. The maximum mean square difference at the end of the optimization routine is usually of the order of 0.001.

HIGH PRECISION CHARACTERIZATION PROCEDURE

S-parameter microwave measurements of chips present serious difficulties for two major reasons :

. The connection reproducibility of the device to the test fixture is usually poor.

. The conventional calibration (3) of Network Analyzers, is not applicable since the usual standards : short-circuit with a minimum series inductance and 50 Ohms loads are not available in a chip form.

These two drawbacks have been overcome by using a coplanar chip carrier for the chips and developing a self calibrating procedure for the measurements.

The Chip Carrier

The GaAs chips used for these measurements have a standard size of 1 X 1 X 0,1 mm. The components to be measured are centered on the chip and have integrated access 50 Ω lines in form of 73,3 µm wide microstrips. Prevision has been made for up the three lines in the case of three port measurements. The chips are mounted on auxiliary 6 X 6 X 0,635 Alumina substrates provided with coplanar tapered 50 Ohms lines (Fig 2). The central ground plane of the coplanar structures acts as a ground plane for the microstrip configuration on the chip.

The Alumina chip carriers are introduced upside down in the test fixture (Fig 3) and connected to the APC 7 - coplanar adapters by pressure contact. The chip carrier insertion takes less than 10 seconds and is highly reproducible. The typical connection reproducibility is given in the table below :

Frequency band 2 - 18 GHz	max amplitude deviation in dB (±)	max phase deviation in degrees (±)
- The same alumina inserted 50 times	0,04*	0,2
- 50 different alumina substrates	0,07	4
- idem after mechanical and electrical selection (40% rejected)	0,04	2

* mainly due to the degradation of the metallisation of the access 50 ohm lines at the transition contact.

The text fixture characteristics with 1 mm long 50 Ω GaAs transmission lines are, (2-18 GHz band) :

- overall VSWR 1,12/1
- losses < 1 dB

The input-output isolation of the test fixture with a GaAs open circuit is better than 40 dB.

- The self calibration procedure (S.C.P.). Since the chip carrier isolation is good, only a ten error model is used to calibrate the test fixture at the chip level.

The procedure (4,5) developed for the calibration of Network Analyzers has been adapted to GaAs microstrip devices.

Three GaAs standards are used to calibrate the measuring system at the centre of the chip :

A through 50 ohm microstrip line of length l_o,
A delay 50 ohm microstrip line of length l_1,
An open circuit line of length $\cong l_o/2$.

The reflexion reference plane is given by the open circuit. The open fringing capacitance ($\cong$ 4,5 fF) has been taken into account (6) by shortening the 50 Ohm access line (- 28 µm). Input and output reference planes are thus located at the center of the chip.

The delay line includes four 45 degree bends with a cornered bevel. Measurements of bevel varying from 0 to 100% have shown that the best value to obtain a minimum v.s.w.r. is 50% in the 2-18 GHz band.

The excess length $l_1 - l_o$ of the delay line when compared to the direct line has to be carrefully chosen to avoid discrepancies at some frequencies. An electrical length of 45 to 60 degrees at the highest frequency proved to give the best results.

- Determination of the complex propagation constant : the redundancy of measured 50 Ω microstrip lines on GaAs gives the value of exp (2 γ ($l_1 - l_o$) where γ is the complex propagation constant. However, the value $l_1 - l_o$ is difficult to evaluate because the elctrical behaviour of the bevels is not exactly known. It is convenient to use a second delay line with the same bevels and a length l_2 which differs from l_1 by an easily measurable value dl.

The S.C.P. procedure gives the relations :

$$\gamma\ (l_1 - l_o) = k_1$$
$$\gamma\ (l_2 - l_o) = k2$$

K_1 and k_2 are known complex constants. In addition we know that :

$$l_2 - l_1 = dl$$

Thus $\gamma = (k_2 - k_1)\ /dl$

The knowledge of λ allows the shift of the calibration planes to any location on the substrate.

- The open circuit reflexion coefficient
The S.C.P. is "self - calibrating", because the exact value of the open (or short) circuit reflexion coefficient has not to be exactly known. No assumption has to be made on the open circuit capacitance or shunt series inductance.

The actual value of the high reflexion coefficient standard (open circuit) can be calculated together with the error terms of the flow graph. This information is used as final test for a good calibration.

The reflexion coefficient of the GaAs open circuit is found to be 1 $\pm$ 0,01 in amplitude and 0 $\pm$ 1 degree in phase from 2 to 18 GHz.

By employing our high precision characterization procedure we characterise passive and active MMIC components on GaAs with a maximum phase and amplitude error of the order of $\pm$ 2 degrees and 1% respectively ; the typical measurement reproducibility if 0,1%.

THEORETICAL AND EXPERIMENTAL CHARACTERIZATION OF SPIRAL INDUCTORS

We have employed the above reported theory in order to evaluate the electrical characteristics of spiral inductor geometries useful for MMIC applications on 100 µm thick GaAs substrates.

The dependence of the inductance (L) on the spiral external diameter (D) is shown in figure 4. For small turn numbers (N = 1,5 to 2,5) the inductance increases almost linearly with the diameter. In th case of larger N-values there is first a non-linear dependence of L = L(D) due to important negative inductive coupling between turn segments of opposite current. This is followed by a linear dependence for higher D values due to the diminution of this coupling at large diameters.

Square spirals with an external side length (a) present smaller inductances than circular spirals with equivalent size diameters.

Inductor values up to 4 nH can be achieved with diameters of the order of 200 µm and N = 3,5.

Fig. 5 shows the parasitic capacitance of circular spirals as a function of D and N. A slightly higher capacitance value is obtained for the outside end of the spirals due to a broader extension of the electrical field. The inside of the spiral is associated with a more confined field, shielded by the outside turns.

For diameter values of the order of magnitude of the substrate thickness and up to about 200 µm the external parasitic capacitance C_{ext} increase almost linearly with the diameter. The same behaviour is observed for the internal parasitic capacitance C_{int} in the case of small turn - numbers. For higher N - values, C_{int} varies in a non-linear way with D due to the increased importance of the capacitance associated with the surface of all intermediate turns.

A study of the influence of the substrate thickness h showed a maximum reduction of 10% for components with D = 200 µm, W = S = 5 µm and N = 1,5 when h changes from 100 to 50 µm. This is followed by an increase of the parasitic capacitance and a negligibly small net variation of the cut-off frequency. The inductor characteristics remain almost constant for thicknesses above 100 µm.

We have realised a large number of spiral inductor geometries by using a mask set with an array having different diameter, width,spacings and number of turns. Air bridges were used for

the connection of the spirals to 50 Ω microstrip input/output lines. The experimental results on the inductors are given in Fig. 6 together with the theoretically predicted values. The inductance is found to increase slightly by approaching the turns to each other due to an increased inductive coupling. A similar increase is observed when the turn width is decreased while the separation is maintened constant. A maximum error of only 5% is found between experiment and theory.

Figures 7 and 8 give the experimental and theoretical cut-off frequency and quality factor data of the inductors. The cut-off frequencies range from 20 to 100 GHz for inductor values smaller than 2 nH.

The quality factor Q can be increased by up to three times by increasing the metallisation thickness as shown in figure 8. This proves that in our case the skin depth is larger than the metal thickness and most of the losses are attributable to the metal resistance.

The experimental procedures permit the accurate evaluation of the parasitic capacitance to earth which is typically 20 fF. This result is found to be in very good accordance with our theory. Our studies demonstrated quality factors of more than 20 at X band for the high inductance value components (∿ 5 nH). Experiments with resonated LC structures confirm these values.

CONCLUSIONS

High precision experimental and theoretical procedures have been developed for obtaining very compact inductors with excellent electrical characteristics. Our experimental procedure permits measurements with a maximum phase and amplitude error. of the order of ± 2 degrees and 1% respectively, while the typical measurement reproducibility is 0.1%.

The new lumped element theory presented in this paper has enabled the prediction of the electrical characteristics of spiral inductors with a maximum error of only 5%. Inductor values up ot 5 nH have been realised and resonant frequencies ranging from 20 to 100 GHz for $L < 2$, nH were obtained. These inductors can be very compact in size (diameter 80 to 200 µm) and are very useful for MMIC's up to mm-wavelengths. An example of an X-band amplifier using these elements will be presented.

The overall conclusion is that since transistors in MMIC's need to be large for different reasons (ease in matching, low noise, high power) with gate widths of 300 to 600 µm, inductors need not be big relatively and can be very useful even at high frequencies.

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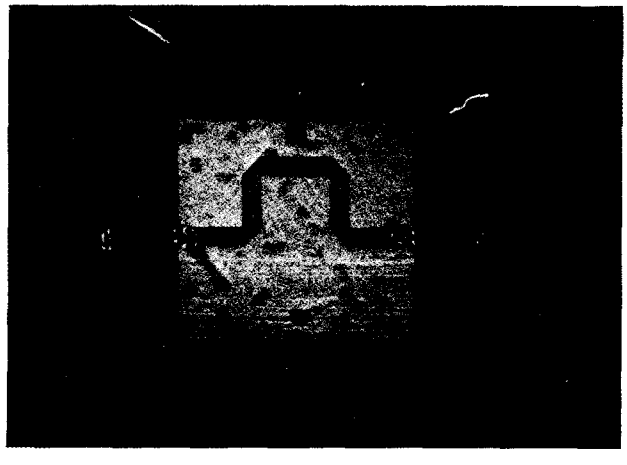

Fig. 2 Alumina Carrier for GaAs Chips

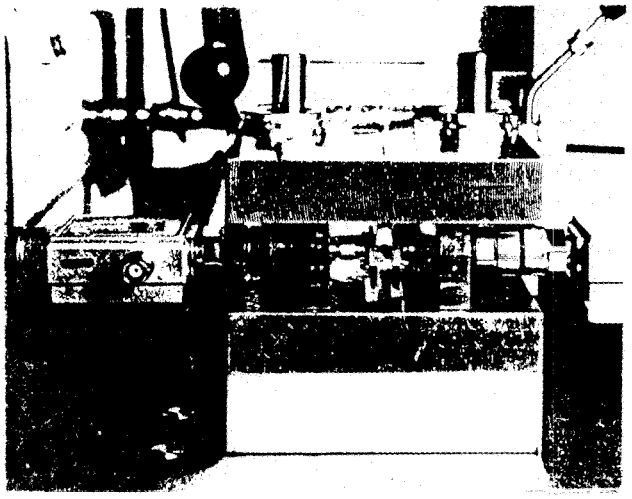

Fig. 3 Test Fixture for Precision Measurements of GaAs Chips

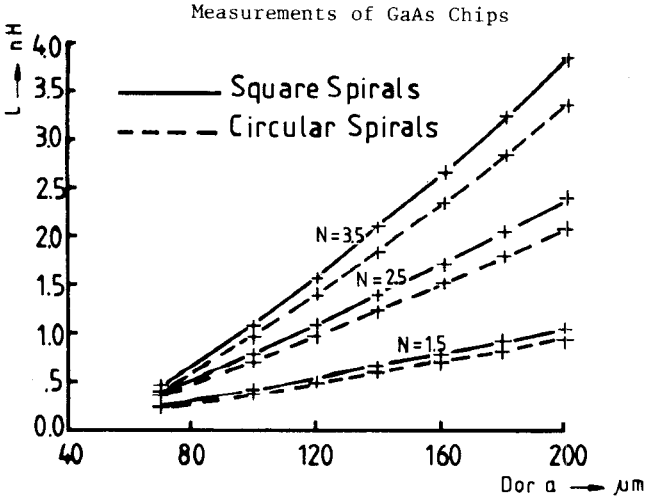

Fig. 4 Theoretical Data for the Inductance (L) of Circular and Square Spirals as a Function of the Diameter (D), Side Length (a) and Number of Turns (N)

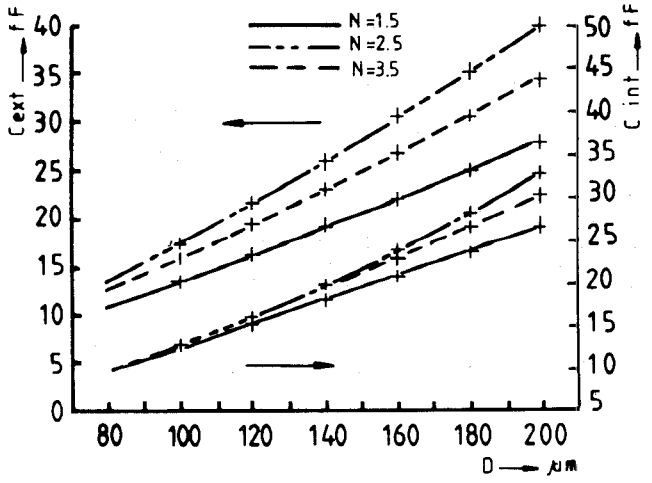

Fig. 5 The Parasitic Capacitance of Circular Spirals (C_{ext}, C_{int}) as a Function of the Diameter (D) and the Number of Turns (N) (Theory)

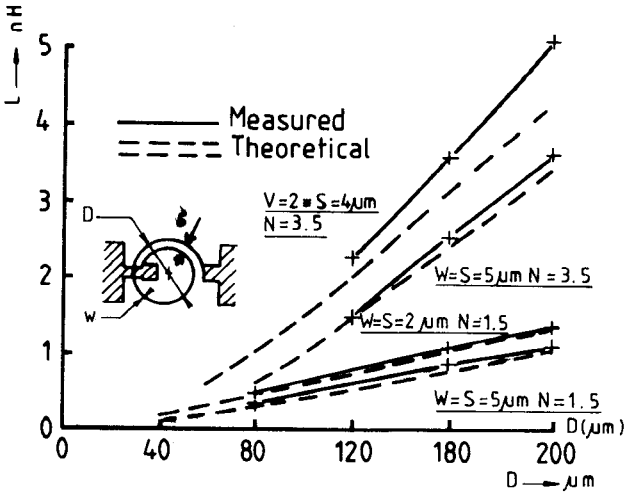

Fig. 6 Experimental and Theoretical Spiral Inductor Characteristics

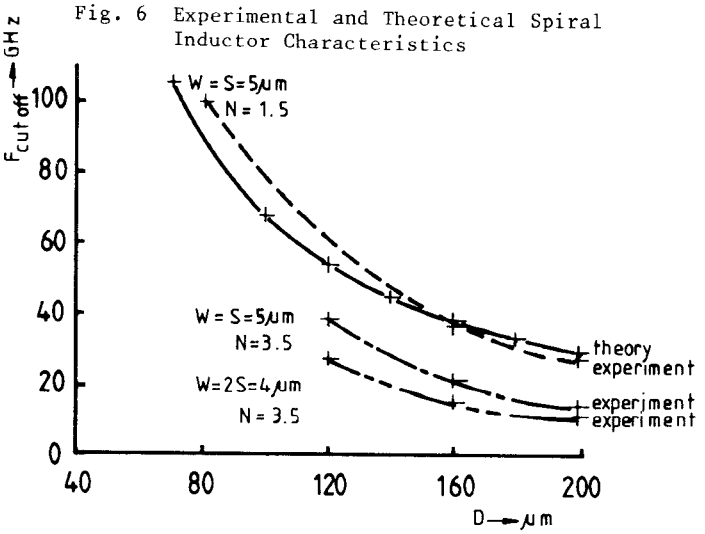

Fig. 7 Cut-Off Frequency Experimental and Theoretical Characteristics of Circular Spirals as a Function of Inductor Diameter

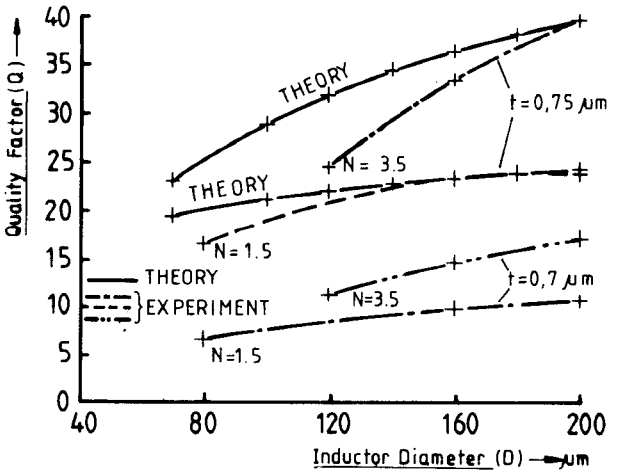

Fig. 8 Experimentally and Theoretically Evaluated Quality Factor Q of Inductors with Different Thickness of Metallisation